REMARKS

Claims 1-11, 13-20, and 22-28 are in the application of which claims 1, 10, 16, and 23 are in independent form.

Specification.

The specification is amended at the paragraph at page 9, line 28 - page 10, line 3 as to add "complementary."

Claim objections. Claims 15, 22, and 27 are objected to because of informalities.

Claim 15 is amended as suggested, but it was noticed that claim 10 upon which claim 15 depends does not refer to full cycle encoded signals, so the word "full" was removed.

Claim 22 is not amended because the specification and drawings give an example. See, for example, Data Out* of FIG. 12.

Claim 27 is not amended because the specification and drawings give an example of not including the complementary cycle encoded signal. See, for example, FIG. 12.

35 U.S.C. 112, first paragraph. Claims 24 and 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

Although it is believed that the claims are definite, claims 24 and 28 are amended to recite: "wherein data is represented in data time segments of the cycle encoded signal."

35 U.S.C. 103(a). Claims 10-11, 14-17, 19-20, 22-23, and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scott et al. (Patent 6,137,827) (hereinafter "Scott") in view of Pfiffner (Patent 5,623,518).

Claims 10 and 23 are amended to recite:

"wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the full cycle encoded signal in response to the data input signal" which is not taught by either Scott or Pfiffner. (Emphasis added.) See, discussion of the multiplexer below in connection with

claim 1.

Claim 16 is amended to recite:

"a delay circuit to delay at least one signal provided by the initial receiving circuit and provide two signals delayed by different amounts and comparison circuitry to compare the two delayed signals, and a logic circuit to receive an output of the comparison circuitry and in response thereto to provide a data out signal which includes recovered data from the full cycle encoded signal."

This is also not taught by either Scott or Pfiffner.

Accordingly, independent claims 10, 16, and 23 should be allowed. Dependent claims 11, 13-15, 17-20, 22, and 24-28 should likewise be allowed for the same reasons. There may be additional reasons for allowing the dependent claims.

35 U.S.C. 103(a). Claims 1-11, 13-20, and 22-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simon et al. (Publication 2001/0006538) (hereinafter "Simon") in view of Pfiffner (Patent 5,623,518).

Claim 1 recites a transmitter in which a full cycle encoded signal is provided by a multiplexer "joining portions of different encoding signals." In particular, claim 1 recites:

"a transmitter including a cycle encoding circuit to receive a data input signal and to provide a full cycle encoded signal in response thereto by continuously joining portions of different encoding signals, * * *;

wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the full cycle encoded signal in response to the data input signal." (Emphasis added.)

These limitations are not taught by either Simon or Pfiffner or the combination of them. In particular, neither Simon nor Pfiffner, nor the combination of them, teaches a multiplexer that receives input data and encoding signals and selects portions of the encoding signals to form a full cycle encoded signal in response to the data input signal.

An example of such a multiplexer in the application is multiplexer 156 in FIG. 4 which selects one of the SF, SF*, SF/2, and SF/2* signals shown in FIG. 5 of the application. Of course, the claims are not limited to the details of these figures.

In Simon, by contrast, there is no such multiplexer. The Office action, page 7, seems to suggest that multiplexer 720 in FIG. 7 of Simon is such a multiplexer stating "multiplexer circuit

720 generates a cycle encoded signal and a complementary cycle ended signal ...." However, for the following reasons, it is not.

1. Multiplexer 720 of Simon does not select portions of encoding signals to form the full cycle encoded signal

Simon describes a system generates symbols that represent more than one bit. For example, paragraph [0086] states:

"[0086] The disclosed embodiment of transmitter 540 modulates a clock signal (CLK_PULSE) to encode four outbound bits per symbol period. One bit is encoded in the symbol's phase (phase bit), two bits are encoded in the symbol's width (width bits) and one bit is encoded in the symbol's amplitude (amplitude bit). * * * " (Emphasis added.)

FIG. 7A shows a circuit used to create the symbol with "a phase modulator 640, pulse-width modulator 630, an amplitude modulator 620 and an output buffer 610." [0082] and [0085]. Paragraphs [0087] - [0089] explain as follows:

[0087] * * * For the disclosed embodiment, the output of phase modulator 640 indicates the leading edge of symbol 420 and serves as a timing reference for generation of the trailing edge by width modulator 630. * * * The output of DMB 714 is a start signal (START), which is provided to amplitude modulator 620 for additional processing.

[0088] Width modulator 630 includes DMs 722, 724, 726, 728, and MUX 720 to generate a second edge that is delayed relative to the first edge by an amount indicated by the width bits. The delayed second edge forms a stop signal (_STOP) that is input to amplitude modulator 620 for additional processing. For the disclosed embodiment of transmitter 540, two bits applied to the control input of MUX 720 select one of four different delays for the second edge, which is provided at the output of MUX 720. Inputs a, b, c, and d of MUX 720 sample the input signal, i.e. the first edge, following its passage through DMs 722, 724, 726, and 728, respectively. If the width bits indicate input c, for example, the second edge output by MUX 720 is delayed by DM 722+DM 724+DM 726 relative to the first edge.

[0089] Amplitude modulator 620 uses START and _STOP to generate a symbol pulse having a first edge, a width, and a polarity indicated by the phase, width, and amplitude bits, respectively, provided to transmitter 540 for a given symbol period. Amplitude modulator 620 includes switches 740(a) and 740(b) which route START to edge-to-pulse generators (EPG) 730(a) and 730(b), respectively, depending on the state of the amplitude bit. Switches 740 may be AND gates, for example. _STOP is provided to second inputs of EPGs 730(a) and 730(b) (generically, EPG 730). On receipt of START, EPG 730 initiates a symbol pulse, which it terminates on receipt of _STOP. Depending on which EPG 730 is activated, a positive or a negative going pulse is provided to the output of transmitter 540 via differential output buffer 610." (Emphasis added.)

Thus, even if the output of edge-to-pulse generators 730(a) and 730(b) could be called

cycle encoded signals and complementary cycle encoded signals (which they cannot), multiplexer 720 does not create the cycle encoded signals. Rather, multiplexer 720 merely provides different delay levels (depending on the value of the width bits) for the STOP signal which is used in the creation of the signals provided by edge-to-pulse generators 730(a) and 730(b).

2. <u>The combination of Simon and Pfiffner does not produce the limitations of claim 1.</u>

Assuming that the signals of FIG 1A of Pfiffner are cycle encoded signals, there is no circuitry Simon that could create them.

As noted above, Simon creates symbols in which four bits are embedded in one symbol. See, Simon, paragraph [0086] quoted above. Further, as noted, the output of multiplexer 720 merely provides different delays for a stop signal. See, Simon, paragraphs [0087] - [0089] quoted above. There is no circuitry in Simon to create a signal like that of FIG. 1A of Pfiffner. The circuitry of Simon would have to be so dramatically altered to create a signal like that in Pfiffner that it would no longer resemble what is in Simon. Therefore, it would not be obvious to combine the teachings of Pfiffner with those of Simon.

Accordingly, the rejection of claim 1 should be withdrawn. Further, for at least the same reasons, the rejections of dependent claims 2-9 should also be withdrawn.

Claims 10 and 23 also recite the multiplexer of claim 1 and should be allowed for the same reason. Dependent claims 11, 13-15, and 24-28 should likewise be allowed for the same reasons. There may be additional reasons for allowing the dependent claims.

Claim 16 is amended to recite:

"a delay circuit to delay at least one signal provided by the initial receiving circuit <u>and provide two signals delayed by different amounts and comparison circuitry to compare the two delayed signals</u>, and a logic circuit to receive <u>an output of the comparison circuitry</u> and in response thereto to provide a data out signal which includes recovered data from the full cycle encoded signal."

Simon and Pfiffner do not teach a delay circuit like this. Accordingly, the rejection of claim 16 should be withdrawn. Further, for at least the same reasons, the rejections of dependent claims 17-20 and 22 should also be withdrawn for the same reason. There may be additional reasons why claims 17-20 and 22 should be allowed.

Accordingly, independent claims 10, 16, and 23 should be allowed. Dependent claims 11, 13-15, 17-20, 22, and 24-28 should likewise be allowed for the same reasons. There may be additional reasons for allowing the dependent claims.

It is noted that there are additional reasons why the claims (such as the dependent claims) are patentable over the cited references.

Allowance of the application is respectfully requested.

Respectfully submitted,

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